## REMARKS

This responds to the Office Action mailed on November 2, 2007.

Claims 7, 12, 14, 15, 22, 29, and 30 are amended, claim 23 is are canceled, and no claims are added; as a result, claims 7, 8, 12, 14, 15, 22, 24, 25 and 29-32 are now pending in this application.

### *§102 Rejection of the Claims*

Claims 7, 8, 12, 13, 22 and 29-32 were rejected under 35 U.S.C. § 102(b) for anticipation by Hughes (US 6,393,536).

Hughes describes a load/store of a scalar processor which uses a buffer to keep track of store memory operations which have probed the data cache. Hughes uses a last-in-buffer indication which identifies whether or not the store in that entry is the youngest store in the buffer to update the memory locations specified by the corresponding store address. Specifically Hughes describes a load/store unit including two buffers, LS1 and LS2, for storing memory operations and two control logics attached to the buffers. The LS1 buffer stores memory operations that have not probed data cache yet. The LS2 buffer stores memory operations after they have been selected to probe the data cache. Hughes, col. 15, lines1-7 and col. 16, lines 61-66.

Hughes' LS2 buffer receives probe status information from data cache 28 for each probe of data cache. The probe status information is stored with its corresponding memory operation in the LS2 buffer. In the case of a memory operation that misses data cache, a miss address buffer (MAB) tag is associated with the LS2 memory operation entry and a cache line corresponding to the memory operation is fetched. When the cache line is returned, the bus interface unit sends the cache line to the data cache and it associated MAB to the LS2 buffer. Load memory operations that match the MAB are then allowed to reprobe the data cache.

Stores which match the MAB tag are marked as hits, but wait to become non-speculative before attempting to commit data.

In contrast, Applicant teaches, and claims in claims 7, 8, 12, 14, 15, 22, 24, 25 and 29-32, using a Force Order Queue (FOQ) to prevent the data cache from satisfying memory requests that match memory operations resident in the FOQ.

Claims 7, 12, 14, 15, 22, 29, and 30 have been amended to emphasize these differences. Reconsideration is respectfully requested.

With regard to claims 8, 9, 11 and 23, these claims are patentable as being dependent on a patentable base claim.

*§103 Rejection of the Claims*

Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes (US 6,393,536) in view of Yamahata (US 5,247,639).

Claims 24 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes.

Claims 14, 15, 24 and 25 are patentable as being dependent on a patentable base claim.

In addition, claim 14 adds the additional requirement that "determining whether a portion of an address associated with the memory request matches one or more partial addresses in an Force Order Queue (FOQ) includes processing the memory request in the FOQ when local cache processing is bypassed." And claim 15 adds the additional requirement that "determining whether a portion of an address associated with the memory request matches one or more partial addresses in an Force Order Queue (FOQ) includes processing the memory request in the FOQ when the memory request includes a synchronization request that causes local cache processing to be bypassed."

Reconsideration and allowance of all remaining claims is respectfully requested.

**Reservation of Rights**

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

## CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date: May 2, 2007

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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 2nd day of May 2007.

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Name

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